

 PALM IntranetApplication  
Number 

IDS Flag Clearance for Application 10775241

**IDS**  
Information

Content	Mailroom Date	Entry Number	IDS Review	Last Modified	Reviewer
<input type="button" value="Update"/>					

## Refine Search

Your wildcard search against 10000 terms has yielded the results below.

***Your result set for the last L# is incomplete.***

The probable cause is use of unlimited truncation. Revise your search strategy to use limited truncation.

### Search Results -

Terms	Documents
L22 AND ((ALTERNAT\$ WITH TRANSMI\$ WITH FRAME) SAME BUS\$) AND (ECU OR (ELECTRIC\$ WITH CONTROL\$ WITH UNIT\$))	1

Database:

US Pre-Grant Publication Full-Text Database  
 US Patents Full-Text Database  
 US OCR Full-Text Database  
 EPO Abstracts Database  
 JPO Abstracts Database  
 Derwent World Patents Index  
 IBM Technical Disclosure Bulletins

Search:

L23

Refine Search

Recall Text

Clear

Interrupt

### Search History

DATE: Monday, December 11, 2006   [Purge Queries](#)   [Printable Copy](#)   [Create Case](#)

<u>Set</u> <u>Name</u> side by side	<u>Query</u>	<u>Hit</u> <u>Count</u>	<u>Set</u> <u>Name</u> result set
	DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; THES=ASSIGNEE; PLUR=YES; OP=OR		
<u>L23</u>	L22 AND ((ALTERNAT\$ WITH TRANSMI\$ WITH FRAME) SAME BUS\$) AND (ECU OR (ELECTRIC\$ WITH CONTROL\$ WITH UNIT\$))	1	<u>L23</u>
<u>L22</u>	L19 OR L20 OR L21 DB=PGPB,USPT; THES=ASSIGNEE; PLUR=YES; OP=OR	65	<u>L22</u>
<u>L21</u>	("20030158649"   "4455654"   "6732044")[URPN]	53	<u>L21</u>
<u>L20</u>	(4339801   4300207   6112152   5995898   4192451   4228537   20030086226   20030221668   4125763)! [PN]	9	<u>L20</u>
<u>L19</u>	("20030158649"   "4455654"   "6732044") [PN] DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; THES=ASSIGNEE; PLUR=YES;	3	<u>L19</u>

OP=OR

<u>L18</u>	L17 AND (ECU OR (ELECTRIC\$ WITH CONTROL\$ WITH UNIT\$))	3	<u>L18</u>
<u>L17</u>	L1 AND L16	53	<u>L17</u>
<u>L16</u>	L14 OR L15	94	<u>L16</u>
<u>L15</u>	((ALTERNAT\$ WITH TRANSMIS\$ WITH FRAME) SAME BUS) AND @PD<=20030219	14	<u>L15</u>
<u>L14</u>	((ALTERNAT\$ WITH TRANSMIS\$ WITH FRAME) SAME BUS) AND @AD<=20030219	91	<u>L14</u>
<u>L13</u>	L11 AND (ECU\$ OR ENG\$ OR ECT\$)	3	<u>L13</u>
<u>L12</u>	L11 AND ECU\$	0	<u>L12</u>
<u>L11</u>	L9 OR L10	20	<u>L11</u>
<u>L10</u>	L6 and @pd<=20030219	20	<u>L10</u>
<u>L9</u>	L6 and @ad<=20030219	19	<u>L9</u>
<u>L8</u>	L6 and diagnos\$	0	<u>L8</u>
<u>L7</u>	L6 and "ECU"	0	<u>L7</u>
<u>L6</u>	L5 and ((simultaneo\$ with "same") with time)	20	<u>L6</u>
<u>L5</u>	L3 and "bus"	124	<u>L5</u>
<u>L4</u>	le and bus	30190	<u>L4</u>
<u>L3</u>	L2 and message	311	<u>L3</u>
<u>L2</u>	L1 and (frame with alternat\$ with transmit\$)	612	<u>L2</u>
<u>L1</u>	communication same frame	113483	<u>L1</u>

END OF SEARCH HISTORY

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L23: Entry 1 of 1

File: USPT

Jun 19, 1984

A US-PAT-NO: 4455654

DOCUMENT-IDENTIFIER: US 4455654 A

**\*\* See image for Certificate of Correction \*\*****\*\* See image for Reexamination Certificate \*\***

TITLE: Test apparatus for electronic assemblies employing a microprocessor

DATE-ISSUED: June 19, 1984

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Bhaskar; Kasi S.	Edmonds	WA		
Carlson; Alden J.	Bothell	WA		
Couper; Alastair N.	Honolulu	HI		
Lambert; Dennis L.	Bothell	WA		
Scott; Marshall H.	Woodinville	WA		

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
John Fluke Mfg. Co., Inc.	Everett	WA			02

APPL-NO: 06/270926 [PALM]

DATE FILED: June 5, 1981

INT-CL-ISSUED: [03] G06F 11/22

## INT-CL-CURRENT:

TYPE IPC	DATE
CIPS <u>G01 R 19/165</u>	20060101
CIPS <u>G01 R 19/165</u>	20060101
CIPN <u>G01 R 31/319</u>	20060101
CIPN <u>G01 R 31/319</u>	20060101
CIPN <u>G01 R 31/28</u>	20060101
CIPN <u>G01 R 31/28</u>	20060101
CIPN <u>G06 F 11/22</u>	20060101
CIPN <u>G06 F 11/22</u>	20060101
CIPN <u>G06 F 11/267</u>	20060101
CIPN <u>G06 F 11/267</u>	20060101
CIPS <u>G06 F 11/26</u>	20060101
CIPS <u>G06 F 11/26</u>	20060101
CIPN <u>G06 F 11/25</u>	20060101
CIPN <u>G06 F 11/25</u>	20060101

CIPS G06 F 11/273 20060101  
CIPS G06 F 11/273 20060101  
CIPN G06 F 11/32 20060101  
CIPN G06 F 11/32 20060101

US-CL-ISSUED: 371/20; 324/73R  
US-CL-CURRENT: 714/28; 714/734

FIELD-OF-CLASSIFICATION-SEARCH: 371/20, 371/25, 371/29, 324/73R, 324/73AT  
See application file for complete search history.

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected

Search ALL

Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<u>4125763</u>	November 1978	Drubing et al.	371/20
<input type="checkbox"/>	<u>4192451</u>	March 1980	Swerling et al.	371/20
<input type="checkbox"/>	<u>4228537</u>	October 1980	Heackels et al.	324/73R X
<input type="checkbox"/>	<u>4300207</u>	November 1981	Eivers et al.	324/73R X
<input type="checkbox"/>	<u>4339801</u>	July 1982	Hosaka et al.	371/20 X

OTHER PUBLICATIONS

Anderson et al. "Processor-Based Tester Goes on Site to Isolate Board Faults Automatically" Electronics May 11, 1978, pp. 111-117.

ART-UNIT: 237

PRIMARY-EXAMINER: Malzahn; David H.

ATTY-AGENT-FIRM: Anable; James W. Ishimaru; Mikio Becker; Stephen A.

ABSTRACT:

A test system for functionally testing and troubleshooting microprocessor-based systems and assemblies is disclosed wherein the test system is connected in place of the microprocessor circuit of the unit being tested (UUT). The test system is itself a microprocessor-based system and includes a microprocessor circuit which is supplied with the UUT clock signal and is the same type of microprocessor circuit as is utilized by the UUT. The test system periodically switches this microprocessor into signal communication with the UUT for a single UUT bus cycle to perform UUT read or write operations. During remaining time periods, the test system microprocessor circuit is in signal communication with the remaining portion of the test system to analyze data obtained from the UUT bus during the previous UUT write or read operation and to establish the signals to be used in the next UUT write or read operation. Various test sequences are provided for testing the UUT bus, RAM, ROM, and write-responsive I/O registers. In addition, a mode of operation

is provided wherein the test system interrogates a fully functional assembly of the type to be tested to derive a memory map and test parameters that permit the test system to perform RAM, ROM, and I/O tests without prior knowledge of the UUT operational sequence or allocation of address space. A test probe provides a visual indication that the logic level at a monitored circuit node is high, low, invalid, or is a sequence of pulses of all three logic levels. The test probe also provides for injection of logical high pulses, logical low pulses or an alternating pulse sequence of high and low pulses. Probe logic level detection and pulse injection can be asynchronous or can be selectively synchronized so that logic level detection or pulse injection occurs with each UUT write or read operation.

56 Claims, 4 Drawing figures

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## Hit List

**First Hit**

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**Search Results - Record(s) 1 through 3 of 3 returned.**

☐ 1. Document ID: US 20030158649 A1

L18: Entry 1 of 3

File: PGPB

Aug 21, 2003

PGPUB-DOCUMENT-NUMBER: 20030158649

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030158649 A1

TITLE: Vehicular electronic control apparatus

PUBLICATION-DATE: August 21, 2003

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Hashimoto, Kohji	Tokyo		JP
Nakamoto, Katsuya	Tokyo		JP

US-CL-CURRENT: 701/114

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw D
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☐ 2. Document ID: US 6732044 B2

L18: Entry 2 of 3

File: USPT

May 4, 2004

US-PAT-NO: 6732044

DOCUMENT-IDENTIFIER: US 6732044 B2

TITLE: Vehicular electronic control apparatus

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw D
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☐ 3. Document ID: US 4455654 A

L18: Entry 3 of 3

File: USPT

Jun 19, 1984

US-PAT-NO: 4455654

DOCUMENT-IDENTIFIER: US 4455654 A

\*\* See image for Certificate of Correction \*\*  
\*\* See image for Reexamination Certificate \*\*

TITLE: Test apparatus for electronic assemblies employing a microprocessor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Abstracts	Abstracts	Claims	KWIC	Draw. De
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Clear	Generate Collection	Print	Fwd Refs	Bkwd Refs	Generate OACS
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Terms	Documents
L17 AND (ECU OR (ELECTRIC\$ WITH CONTROL\$ WITH UNIT\$))	3

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Search Results - Record(s) 1 through 10 of 20 returned.

☐ 1. Document ID: US 6522634 B1

L6: Entry 1 of 20

File: USPT

Feb 18, 2003

US-PAT-NO: 6522634

DOCUMENT-IDENTIFIER: US 6522634 B1

TITLE: Wireless transmission system.

Full	Title	Citation	Front	Review	Classification	Date	Reference	Spoliers	Attachments	Claims	KMIC	Draw De
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☐ 2. Document ID: US 6388997 B1

L6: Entry 2 of 20

File: USPT

May 14, 2002

US-PAT-NO: 6388997

DOCUMENT-IDENTIFIER: US 6388997 B1

**\*\* See image for Certificate of Correction \*\***

TITLE: Timing adjustment control for efficient time division duplex communication

Full	Title	Citation	Front	Review	Classification	Date	Reference	Spoliers	Attachments	Claims	KMIC	Draw De
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☐ 3. Document ID: US 6381239 B1

L6: Entry 3 of 20

File: USPT

Apr 30, 2002

US-PAT-NO: 6381239

DOCUMENT-IDENTIFIER: US 6381239 B1

TITLE: Multiple application switching platform and method

Full	Title	Citation	Front	Review	Classification	Date	Reference	Spoliers	Attachments	Claims	KMIC	Draw De
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☐ 4. Document ID: US 6366566 B1

L6: Entry 4 of 20

File: USPT

Apr 2, 2002

US-PAT-NO: 6366566

DOCUMENT-IDENTIFIER: US 6366566 B1

TITLE: Efficient communication system using time division multiplexing and timing adjustment control

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 5. Document ID: US 6338105 B1

L6: Entry 5 of 20

File: USPT

Jan 8, 2002

US-PAT-NO: 6338105

DOCUMENT-IDENTIFIER: US 6338105 B1

TITLE: Data transmission method and game system constructed by using the method

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 6. Document ID: US 6324603 B1

L6: Entry 6 of 20

File: USPT

Nov 27, 2001

US-PAT-NO: 6324603

DOCUMENT-IDENTIFIER: US 6324603 B1

TITLE: Data transmission system and game system using the same

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 7. Document ID: US 6213879 B1

L6: Entry 7 of 20

File: USPT

Apr 10, 2001

US-PAT-NO: 6213879

DOCUMENT-IDENTIFIER: US 6213879 B1

TITLE: Data transmission system and game system with game peripherals using same

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 8. Document ID: US 6094421 A

L6: Entry 8 of 20

File: USPT

Jul 25, 2000

US-PAT-NO: 6094421

DOCUMENT-IDENTIFIER: US 6094421 A

TITLE: Timing adjustment control for efficient time division duplex, frequency division duplex or hybrid time division duplex/frequency division duplex communication

Full	Title	Citation	Front	Review	Classification	Date	Reference	References	Attachments	Claims	KWIC	Draw De
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☐ 9. Document ID: US 6049538 A

L6: Entry 9 of 20

File: USPT

Apr 11, 2000

US-PAT-NO: 6049538

DOCUMENT-IDENTIFIER: US 6049538 A

**\*\* See image for Certificate of Correction \*\***

TITLE: Efficient communication system using time division multiplexing and timing adjustment control

Full	Title	Citation	Front	Review	Classification	Date	Reference	References	Attachments	Claims	KWIC	Draw De
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☐ 10. Document ID: US 5959980 A

L6: Entry 10 of 20

File: USPT

Sep 28, 1999

US-PAT-NO: 5959980

DOCUMENT-IDENTIFIER: US 5959980 A

TITLE: Timing adjustment control for efficient time division duplex communication

Full	Title	Citation	Front	Review	Classification	Date	Reference	References	Attachments	Claims	KWIC	Draw De
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Terms

Documents

L5 and ((simultaneo\$ with "same") with time)

20

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Search Results - Record(s) 11 through 20 of 20 returned.

☐ 11. Document ID: US 5802046 A

L6: Entry 11 of 20

File: USPT

Sep 1, 1998

US-PAT-NO: 5802046

DOCUMENT-IDENTIFIER: US 5802046 A

TITLE: Efficient time division duplex communication system with interleaved format and timing adjustment control

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequence	Attachment	Claims	KWIC	Draw De
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☐ 12. Document ID: US 5745484 A

L6: Entry 12 of 20

File: USPT

Apr 28, 1998

US-PAT-NO: 5745484

DOCUMENT-IDENTIFIER: US 5745484 A

TITLE: Efficient communication system using time division multiplexing and timing adjustment control

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequence	Attachment	Claims	KWIC	Draw De
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☐ 13. Document ID: US 5689502 A

L6: Entry 13 of 20

File: USPT

Nov 18, 1997

US-PAT-NO: 5689502

DOCUMENT-IDENTIFIER: US 5689502 A

TITLE: Efficient frequency division duplex communication system with interleaved format and timing adjustment control

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequence	Attachment	Claims	KWIC	Draw De
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☐ 14. Document ID: US 5416780 A

L6: Entry 14 of 20

File: USPT

May 16, 1995

US-PAT-NO: 5416780

DOCUMENT-IDENTIFIER: US 5416780 A

TITLE: Telecommunications system and protocol for avoiding message collisions on a multiplexed communications link

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 15. Document ID: US 5406627 A

L6: Entry 15 of 20

File: USPT

Apr 11, 1995

US-PAT-NO: 5406627

DOCUMENT-IDENTIFIER: US 5406627 A

**\*\* See image for Reexamination Certificate \*\***

TITLE: Digital data cryptographic system

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 16. Document ID: US 5267312 A

L6: Entry 16 of 20

File: USPT

Nov 30, 1993

US-PAT-NO: 5267312

DOCUMENT-IDENTIFIER: US 5267312 A

TITLE: Audio signal cryptographic system

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 17. Document ID: US 5185794 A

L6: Entry 17 of 20

File: USPT

Feb 9, 1993

US-PAT-NO: 5185794

DOCUMENT-IDENTIFIER: US 5185794 A

TITLE: System and method for scrambling and/or descrambling a video signal

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 18. Document ID: US 5166976 A

L6: Entry 18 of 20

File: USPT

Nov 24, 1992

US-PAT-NO: 5166976

DOCUMENT-IDENTIFIER: US 5166976 A

TITLE: System and method for detection of a pulse within a video signal

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 19. Document ID: US 5091938 A

L6: Entry 19 of 20

File: USPT

Feb 25, 1992

US-PAT-NO: 5091938

DOCUMENT-IDENTIFIER: US 5091938 A

**\*\* See image for Reexamination Certificate \*\***

TITLE: System and method for transmitting entertainment information to authorized ones of plural receivers

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMCC	Draw De
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☐ 20. Document ID: US 2235803 A

L6: Entry 20 of 20

File: USOC

Mar 18, 1941

US-PAT-NO: 2235803

DOCUMENT-IDENTIFIER: US 2235803 A

TITLE: Telephone system

DATE-ISSUED: March 18, 1941

INVENTOR-NAME: CARPENTER WARREN W

US-CL-CURRENT: 379/32.04; 379/221.01, 379/275

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMCC	Draw De
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Terms	Documents
L5 and ((simultaneo\$ with "same") with time).	20

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Print

L23: Entry 1 of 1

File: USPT

Jun 19, 1984

DOCUMENT-IDENTIFIER: US 4455654 A

\*\* See image for [Certificate of Correction](#) \*\*\*\* See image for [Reexamination Certificate](#) \*\*

TITLE: Test apparatus for electronic assemblies employing a microprocessor

Detailed Description Text (6):

As shall be described in more detail hereinafter, during the various test sequences that are performed in accordance with this invention, switch 38 is activated to sequentially switch microprocessor circuit 42 between the pod processor state and the UUT test state. Basically, this alternating sequence is utilized so that microprocessor circuit 42: (a) first operates in the pod processor state (i.e., in conjunction with pod ROM 48 and pod RAM 50) to determine the next test instruction to be carried out and the associated UUT stimulus (e.g., an instruction to write a specific word of data at a particular address of UUT RAM 26); (b) switches to the UUT test state to couple the test stimulus to UUT 18 (e.g., write the desired data word at the specified address of UUT RAM 26) and to latch signals into drivability register 40 that are representative of the logic levels on UUT bus 32 at the conclusion of the UUT test state; and (c) switches back to the pod processor state for the analysis of the data stored in drivability register 40 and the formation of the next test instruction and stimulus and/or transmission of a signal to main frame 10 (via pod I/O unit 52) which indicates the result of the test step that was just completed.

Detailed Description Text (15):

Probe control and measurement unit 92 is electrically connected to a probe unit 94, which is utilized both as a means of injecting and measuring logic signals at a selected circuit node of UUT 18 when detailed troubleshooting or fault isolation procedures are being implemented with this invention (i.e., after performing the various hereinafter test sequences which generally localize a fault or failure to a particular portion of the UUT circuitry). As shall be discussed relative to the various test sequences that are typically employed with the invention and with respect to the realization of a probe control and measurement and that is illustrated in FIG. 3, complete troubleshooting routines that utilize probe 94 can be stored in the read-only memory circuits of main frame 10 and interface pod 12 (pod ROM 48 and main frame ROM 98) or such programs can be loaded into mass memory 82 from keyboard 88 or conventional data storage apparatus employing tape or other storage media. Additionally, the presently-preferred embodiments of the invention permit probe unit 94 to be used, in effect, as a separate test instrument (i.e., without the execution of a supporting test sequence that is designed for the particular type of UUT being tested). When utilized in such a manner, probe 94 can be used to perform various well-known troubleshooting techniques ranging from simple logic level sensing to transition counting and the type of cyclic redundancy check that is commonly referred to as "signature analysis" when used in conjunction with the pod stimulus capability.

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Search Results - Record(s) 1 through 9 of 9 returned.

☐ 1. Document ID: US 20030221668 A1

L24: Entry 1 of 9

File: PGPB

Dec 4, 2003

PGPUB-DOCUMENT-NUMBER: 20030221668

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030221668 A1

TITLE: On-vehicle engine control apparatus

PUBLICATION-DATE: December 4, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Hashimoto, Kohji	Tokyo		JP
Nakamoto, Katsuya	Tokyo		JP

US-CL-CURRENT: 123/396; 123/399

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 2. Document ID: US 20030158649 A1

L24: Entry 2 of 9

File: PGPB

Aug 21, 2003

PGPUB-DOCUMENT-NUMBER: 20030158649

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030158649 A1

TITLE: Vehicular electronic control apparatus

PUBLICATION-DATE: August 21, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Hashimoto, Kohji	Tokyo		JP
Nakamoto, Katsuya	Tokyo		JP

US-CL-CURRENT: 701/114

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw De
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☐ 3. Document ID: US 20030086226 A1

L24: Entry 3 of 9

File: PGPB

May 8, 2003

PGPUB-DOCUMENT-NUMBER: 20030086226

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20030086226 A1

TITLE: On-vehicle electronic control device

PUBLICATION-DATE: May 8, 2003

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY
Hashimoto, Kohji	Tokyo		JP
Nakamoto, Katsuya	Tokyo		JP
Watanabe, Tetsushi	Tokyo		JP
Yamashita, Manabu	Tokyo		JP

US-CL-CURRENT: 361/91.1

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC	Draw De
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☐ 4. Document ID: US 6732044 B2

L24: Entry 4 of 9

File: USPT

May 4, 2004

US-PAT-NO: 6732044

DOCUMENT-IDENTIFIER: US 6732044 B2

TITLE: Vehicular electronic control apparatus

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC	Draw De
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☐ 5. Document ID: US 6559671 B2

L24: Entry 5 of 9

File: USPT

May 6, 2003

US-PAT-NO: 6559671

DOCUMENT-IDENTIFIER: US 6559671 B2

TITLE: Efficient parallel testing of semiconductor devices using a known good device to generate expected responses

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KMC	Draw De
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☐ 6. Document ID: US 6112152 A

L24: Entry 6 of 9

File: USPT

Aug 29, 2000

US-PAT-NO: 6112152

DOCUMENT-IDENTIFIER: US 6112152 A

**\*\* See image for Certificate of Correction \*\***TITLE: RFID system in communication with vehicle on-board computer

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KVMC	Draw De
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☐ 7. Document ID: US 5995898 A

L24: Entry 7 of 9

File: USPT

Nov 30, 1999

US-PAT-NO: 5995898

DOCUMENT-IDENTIFIER: US 5995898 A

**\*\* See image for Certificate of Correction \*\***TITLE: RFID system in communication with vehicle on-board computer

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KVMC	Draw De
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☐ 8. Document ID: US 4639901 A

L24: Entry 8 of 9

File: USPT

Jan 27, 1987

US-PAT-NO: 4639901

DOCUMENT-IDENTIFIER: US 4639901 A

TITLE: Method for testing cableless seismic digital field recorders

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KVMC	Draw De
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☐ 9. Document ID: US 4339801 A

L24: Entry 9 of 9

File: USPT

Jul 13, 1982

US-PAT-NO: 4339801

DOCUMENT-IDENTIFIER: US 4339801 A

TITLE: Automatic control system for method and apparatus for checking devices of an automotive vehicle in use with a microcomputer

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KVMC	Draw De
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Bkwd Refs

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L22 AND (CAR OR VEHICLE OR AUTOMOBILE)

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L24: Entry 4 of 9

File: USPT

May 4, 2004

US-PAT-NO: 6732044

DOCUMENT-IDENTIFIER: US 6732044 B2

TITLE: Vehicular electronic control apparatus

DATE-ISSUED: May 4, 2004

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hashimoto; Kohji	Tokyo			JP
Nakamoto; Katsuya	Tokyo			JP

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Mitsubishi Denki Kabushiki Kaisha	Tokyo			JP	03

APPL-NO: 10/212045 [PALM]

DATE FILED: August 6, 2002

## FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	P2002-043850	February 20, 2002

INT-CL-ISSUED: [07] G06F 13/12, G06F 11/00

## INT-CL-CURRENT:

TYPE	IPC	DATE
CIPS	<u>F02 D 41/26</u>	20060101
CIPS	<u>F02 D 41/00</u>	20060101

US-CL-ISSUED: 701/114; 701/115, 701/102, 701/1

US-CL-CURRENT: 701/114; 701/1, 701/102, 701/115FIELD-OF-CLASSIFICATION-SEARCH: 701/114, 701/115, 701/102, 701/1, 701/29, 701/43  
See application file for complete search history.

## PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/> <u>5995898</u>	November 1999	Tuttle	701/102
<input type="checkbox"/> <u>6112152</u>	August 2000	Tuttle	701/115
<input type="checkbox"/> <u>2003/0086226</u>	May 2003	Hashimoto et al.	361/91.1
<input type="checkbox"/> <u>2003/0221668</u>	December 2003	Hashimoto et al.	123/396

## FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	CLASS
o 666 199	August 1995	EP	
5-81222	April 1993	JP	
5-119811	May 1993	JP	
7-13912	January 1995	JP	
7-196003	August 1995	JP	
8-305681	November 1996	JP	
8-339308	December 1996	JP	
9-83301	March 1997	JP	
2000-68833	March 2000	JP	
2000-89974	March 2000	JP	

ART-UNIT: 3747

PRIMARY-EXAMINER: Vo; Hieu T.

ATTY-AGENT-FIRM: Sugrue Mion, PLLC

## ABSTRACT:

A core integrated circuit device has a microprocessor. A first ancillary integrated circuit device has an indirect parallel input circuit that receives low-speed digital signals parallel, and the first ancillary integrated circuit device outputs the received digital signals serially to the core integrated circuit device. A second ancillary integrated circuit device has a multi-channel A/D converter that receives analog signals parallel and converts those into digital signals, and the second ancillary integrated circuit device outputs the digital signals serially to the core integrated circuit device. The core integrated circuit device generates control signals based on the received signals and outputs the control signals to control object devices.

19 Claims, 19 Drawing figures

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L24: Entry 5 of 9

File: USPT

May 6, 2003

US-PAT-NO: 6559671

DOCUMENT-IDENTIFIER: US 6559671 B2

TITLE: Efficient parallel testing of semiconductor devices using a known good device to generate expected responses

DATE-ISSUED: May 6, 2003

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Miller; Charles A.	Fremont	CA		
Roy; Richard S.	Danville	CA		

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
FormFactor, Inc.	Livermore	CA			02

APPL-NO: 10/208173 [\[PALM\]](#)

DATE FILED: July 29, 2002

## PARENT-CASE:

This is a Continuation application of Ser. No. 09/260,460, filed Mar. 1, 1999 now U.S. Pat. No. 6,452,411. The subject matter in this application is related to material in two other U.S. patent applications of Roy and Miller, entitled DISTRIBUTED INTERFACE FOR PARALLEL TESTING OF MULTIPLE DEVICES USING A SINGLE TESTER CHANNEL, having Ser. No. 09/260,463 (pending), and PARALLEL TESTING OF INTEGRATED CIRCUIT DEVICES USING CROSS-DUT AND WITHIN-DUT COMPARISONS, having Ser. No. 09/260,459 now U.S. Pat. No. 6,480,978, filed on the same date as this application and expressly incorporated herein by reference.

INT-CL-ISSUED: [07] G01R 31/26, G01R 31/28

## INT-CL-CURRENT:

TYPE IPC	DATE
CIPS <a href="#">G01 R 31/319</a>	20060101
CIPS <a href="#">G01 R 31/3193</a>	20060101
CIPS <a href="#">G01 R 31/28</a>	20060101

US-CL-ISSUED: 324/765; 714/736, 702/119

US-CL-CURRENT: [324/765](#); [702/119](#), [714/736](#)

FIELD-OF-CLASSIFICATION-SEARCH: 324/158.1, 324/765, 702/117-120, 714/714, 714/719, 714/733, 714/735, 714/736, 714/737

See application file for complete search history.

PRIOR-ART-DISCLOSED:

## U.S. PATENT DOCUMENTS

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<u>3821645</u>	June 1974	Vinsani	
<input type="checkbox"/>	<u>4370746</u>	January 1983	Jones et al.	
<input type="checkbox"/>	<u>4455654</u>	June 1984	Bhaskar et al.	
<input type="checkbox"/>	<u>4773028</u>	September 1988	Tallman	
<input type="checkbox"/>	<u>4942576</u>	July 1990	Busack et al.	
<input type="checkbox"/>	<u>5070297</u>	December 1991	Kwon et al.	
<input type="checkbox"/>	<u>5243274</u>	September 1993	Kelsey et al.	
<input type="checkbox"/>	<u>5357523</u>	October 1994	Bogholtz, Jr. et al.	
<input type="checkbox"/>	<u>5363038</u>	November 1994	Love	
<input type="checkbox"/>	<u>5442282</u>	August 1995	Rostoker et al.	
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<input type="checkbox"/>	<u>5689515</u>	November 1997	Panis	
<input type="checkbox"/>	<u>5701666</u>	December 1997	DeHaven et al.	
<input type="checkbox"/>	<u>5794175</u>	August 1998	Conner	
<input type="checkbox"/>	<u>5839100</u>	November 1998	Wegener	
<input type="checkbox"/>	<u>5910895</u>	June 1999	Proskauer et al.	
<input type="checkbox"/>	<u>5923178</u>	July 1999	Higgins et al.	
<input type="checkbox"/>	<u>5995424</u>	November 1999	Lawrence et al.	
<input type="checkbox"/>	<u>5995915</u>	November 1999	Reed et al.	
<input type="checkbox"/>	<u>6064213</u>	May 2000	Khandros	
<input type="checkbox"/>	<u>6064948</u>	May 2000	West et al.	
<input type="checkbox"/>	<u>6246250</u>	June 2001	Doherty et al.	
<input type="checkbox"/>	<u>6256760</u>	July 2001	Carron et al.	
<input type="checkbox"/>	<u>6275962</u>	August 2001	Fuller et al.	
<input type="checkbox"/>	<u>6324665</u>	November 2001	Fay	714/736

## FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	CLASS
61099876	May 1986	JP	
6027195	April 1994	JP	

## OTHER PUBLICATIONS

"N-UP Test Adapter," IBM Technical Disclosure Bulletin, vol. 39, No. 7 (Jul. 1996), pp. 243-244.

ART-UNIT: 2829

PRIMARY-EXAMINER: Cuneo; Kamand

ASSISTANT-EXAMINER: Kobert; Russell M.

ATTY-AGENT-FIRM: Burraston; N. Kenneth Merkadeau; Stuart L.

## ABSTRACT:

A system for testing integrated circuit devices is disclosed in which a tester communicates with a known good device through a channel. Tester-DUT interface circuitry is provided for monitoring the channel while the tester is writing data as part of a test sequence to locations in the known good device. In response, the interface circuitry writes the data to corresponding locations in each of a number of devices under test (DUTs). The interface circuitry monitors the channel while the tester is reading from the locations in the known good device (KGD), and in response performs a comparison between DUT data read from the corresponding locations in the DUTs and expected responses obtained from the KGD.

5 Claims, 5 Drawing figures

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File: USPT

Aug 29, 2000

US-PAT-NO: 6112152

DOCUMENT-IDENTIFIER: US 6112152 A

**\*\* See image for Certificate of Correction \*\***TITLE: RFID system in communication with vehicle on-board computer

DATE-ISSUED: August 29, 2000

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Tuttle; John R.	Boise	ID		

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Micron Technology, Inc.	Boise	ID			02

APPL-NO: 09/378435 [PALM]

DATE FILED: August 20, 1999

## PARENT-CASE:

CROSS REFERENCE TO RELATED APPLICATION This is a Continuation of U.S. patent application Ser. No. 08/759,737, filed Dec. 6, 1996, now U.S. Pat. No. 5,995,898, Issued Nov. 30, 1999, and titled "RFID System in Communication with Vehicle On-Board Computer".

INT-CL-ISSUED: [07] G08G 1/017, G07C 5/00, G06F 13/00, H04L 9/00

## INT-CL-CURRENT:

TYPE IPC	DATE
CIPS <u>G07 C 5/00</u>	20060101
CIPS <u>G08 G 1/0962</u>	20060101
CIPS <u>G08 G 1/0967</u>	20060101
CIPS <u>G08 G 1/095</u>	20060101
CIPS <u>G07 C 5/08</u>	20060101
CIPS <u>G08 G 1/017</u>	20060101
CIPS <u>G07 B 15/00</u>	20060101

US-CL-ISSUED: 701/115; 701/101, 701/102, 701/114, 701/117, 340/348, 340/825.34

US-CL-CURRENT: 701/115; 340/5.61, 701/101, 701/102, 701/114, 701/117

FIELD-OF-CLASSIFICATION-SEARCH: 701/102, 701/114, 701/101, 701/33, 701/115, 701/117, 340/438, 340/991, 340/933, 340/539, 340/825.34, 455/546  
See application file for complete search history.

## PRIOR-ART-DISCLOSED:



## U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<u>4072850</u>	February 1978	McGlynn	701/35
<input type="checkbox"/>	<u>4075632</u>	February 1978	Baldwin et al.	343/6.8
<input type="checkbox"/>	<u>4107689</u>	August 1978	Jellinek	340/991
<input type="checkbox"/>	<u>4168679</u>	September 1979	Ikeura et al.	123/32
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<input type="checkbox"/>	<u>4551803</u>	November 1985	Hosaka et al.	701/115
<input type="checkbox"/>	<u>4552116</u>	November 1985	Kuroiwa et al.	123/489
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<input type="checkbox"/>	<u>4843557</u>	June 1989	Ina et al.	364/431.11
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<input type="checkbox"/>	<u>4875391</u>	October 1989	Leising et al.	74/866
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<input type="checkbox"/>	<u>4908792</u>	March 1990	Przybyla et al.	364/900
<input type="checkbox"/>	<u>4926182</u>	May 1990	Ohta et al.	342/44
<input type="checkbox"/>	<u>4986229</u>	January 1991	Suzuki et al.	123/179
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<input type="checkbox"/>	<u>5058044</u>	October 1991	Stewart et al.	340/825.54
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<input type="checkbox"/>	<u>5150609</u>	September 1992	Ebner et al.	73/117.3
<input type="checkbox"/>	<u>5172321</u>	December 1992	Ghaem et al.	364/444.2
<input type="checkbox"/>	<u>5189612</u>	February 1993	Lemercier et al.	364/424.02
<input type="checkbox"/>	<u>5196846</u>	March 1993	Brockelsby et al.	340/933
<input type="checkbox"/>	<u>5278759</u>	January 1994	Berra et al.	364/424.01
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<input type="checkbox"/>	<u>5610574</u>	March 1997	Motoh et al.	340/426
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<input type="checkbox"/>	<u>5621380</u>	April 1997	Mutoh et al.	340/426
<input type="checkbox"/>	<u>5621381</u>	April 1997	Kawachi et al.	342/51
<input type="checkbox"/>	<u>5621412</u>	April 1997	Sharpe et al.	342/51
<input type="checkbox"/>	<u>5631501</u>	May 1997	Kubota et al.	307/10.5
<input type="checkbox"/>	<u>5634190</u>	May 1997	Wiedman	455/13.1
<input type="checkbox"/>	<u>5635693</u>	June 1997	Benson et al.	340/825.54
<input type="checkbox"/>	<u>5649296</u>	July 1997	MacLellan et al.	455/38.2
<input type="checkbox"/>	<u>5660246</u>	August 1997	Kaman	180/287
<input type="checkbox"/>	<u>5664113</u>	September 1997	Worger et al.	705/28
<input type="checkbox"/>	<u>5677667</u>	October 1997	Lesesky et al.	340/431
<input type="checkbox"/>	<u>5686920</u>	November 1997	Hurta et al.	342/42
<input type="checkbox"/>	<u>5710703</u>	January 1998	Kirn et al.	364/424.034
<input type="checkbox"/>	<u>5712899</u>	January 1998	Pace, II	379/58
<input type="checkbox"/>	<u>5717830</u>	February 1998	Sigler et al.	455/426
<input type="checkbox"/>	<u>5719550</u>	February 1998	Bloch et al.	340/426
<input type="checkbox"/>	<u>5721678</u>	February 1998	Widl	364/424.04
<input type="checkbox"/>	<u>5724426</u>	March 1998	Rosenow et al.	380/25
<input type="checkbox"/>	<u>5726630</u>	March 1998	Marsh et al.	340/572
<input type="checkbox"/>	<u>5729538</u>	March 1998	Dent	370/347
<input type="checkbox"/>	<u>5729740</u>	March 1998	Tsumura	395/615
<input type="checkbox"/>	<u>5749984</u>	May 1998	Frey et al.	340/444
<input type="checkbox"/>	<u>5758300</u>	May 1998	Abe	455/456
<input type="checkbox"/>	<u>5769051</u>	June 1998	Bayron et al.	123/335
<input type="checkbox"/>	<u>5803043</u>	September 1998	Bayron et al.	123/335
<input type="checkbox"/>	<u>5809142</u>	September 1998	Hurta et al.	380/24
<input type="checkbox"/>	<u>5894266</u>	April 1999	Wood, Jr. et al.	340/539
<input type="checkbox"/>	<u>5995898</u>	November 1999	Tuttle	701/102
	<u>6006148</u>	December 1999	Strong	701/33



## FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	CLASS
0 456 425	May 1991	EP	
0 725 377	August 1996	EP	
2 647 930	June 1989	FR	
3445668	December 1984	DE	
2 169 173	July 1986	GB	
2277844	November 1994	GB	
WO 90/12365	October 1990	WO	
WO 91/18452	November 1991	WO	
WO 93/04353	March 1993	WO	
WO 94/07206	March 1994	WO	
WO 95/01607	January 1995	WO	
98/25248	June 1998	WO	

## OTHER PUBLICATIONS

"Engine Air Control--Basis of a Vehicular Systems Control Hierarchy", Donald L. Stivender, Society of Automotive Engineers, Inc., 1978.

ART-UNIT: 377

PRIMARY-EXAMINER: Yuen; Henry C.

ASSISTANT-EXAMINER: Vo; Hieu T.

ATTY-AGENT-FIRM: Wells, St. John, Roberts, Gregory & Matkin, P.S.

## ABSTRACT:

A system comprising a vehicle on-board computer; and a wireless transponder device coupled to the vehicle on-board computer. The system performs a variety of functions because of its ability to transmit and receive data from other transponders which may be remote from the vehicle or located in the vehicle at a location spaced apart from the system. Remote transponders are spaced apart from the vehicle. The remote transponders can be positioned, for example, at a gas station, toll booth, service center, dealership, parking lot, or along a roadside.

41 Claims, 4 Drawing figures

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File: USPT

Jul 13, 1982

US-PAT-NO: 4339801

DOCUMENT-IDENTIFIER: US 4339801 A

TITLE: Automatic control system for method and apparatus for checking devices of an automotive vehicle in use with a microcomputer

DATE-ISSUED: July 13, 1982

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hosaka; Akio	Yokohama			JP
Higashiyama; Kazuhiro	Atsugi			JP

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Nissan Motor Company, Limited	Yokohama			JP	03

APPL-NO: 06/132647 [PALM]

DATE FILED: March 21, 1980

INT-CL-ISSUED: [03] G06F 11/00

## INT-CL-CURRENT:

TYPE IPC	DATE
CIPS <u>F02 D 41/00</u>	20060101
CIPS <u>F02 D 41/26</u>	20060101
CIPS <u>G06 F 11/277</u>	20060101
CIPS <u>G06 F 11/273</u>	20060101
CIPS <u>G06 F 11/27</u>	20060101

US-CL-ISSUED: 364/431.04; 371/16, 371/20, 371/21, 123/417, 123/480

US-CL-CURRENT: 701/102; 123/480, 714/719, 714/722

FIELD-OF-CLASSIFICATION-SEARCH: 371/16, 371/20, 371/21, 364/431, 123/416, 123/417, 123/479, 123/480

See application file for complete search history.

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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<input type="checkbox"/>	<u>3838264</u>	September 1974	Maker	371/21
<input type="checkbox"/>	<u>4034194</u>	July 1977	Thomas et al.	371/20
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<input type="checkbox"/>	<u>4158431</u>	June 1979	Van Bavel et al.	371/20
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<input type="checkbox"/>	<u>4255789</u>	March 1981	Hartford et al.	364/431
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2756719	July 1978	DE	
2726115	December 1978	DE	
1437217	May 1976	GB	
1459851	December 1976	GB	
1480520	July 1977	GB	
1504096	March 1978	GB	

ART-UNIT: 236

PRIMARY-EXAMINER: Atkinson, Charles E.

ATTY-AGENT-FIRM: Schwartz, Jeffery, Schwaab, Mack, Blumenthal &amp; Koch

## ABSTRACT:

An automatic control system for an automotive vehicle in use with a microcomputer has a checking system for checking an input unit, a ROM, a RAM and an output unit of the microcomputer. The checking system comprises a means which stores various checking programs to be executed for checking above-mentioned elements of the microcomputer. The checking system effectively operates to check the elements without causing expanding of duration of execution of the checking programs.

9 Claims, 19 Drawing figures